Approved in 52nd BoA Meeting(02.11.2023)

IIT Mandi
Proposal for a New Course

Course number : EE326
Course Name : Computer Organization and Processor Architecture Design
Credit : 3-0-2-4
Distribution : Odd/Even
Intended for : B. Tech in Electrical Engineering
Prerequisite : Digital System Design (EE210) or equivalent

Mutual Exclusion: Computer Organization (CS201)

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1. Preamble:

This course provides an introduction to the design and implementation of basic building blocks of a computer at a logic circuit level with special emphasis on microprocessor design. The course assumes a previous course on digital logic design. The course aims at providing a *designers' perspective to a computer system*. Students are expected to model the computer hardware using a hardware description language with the target of modelling and simulating a typical processor.

2. Course Modules with quantitative lecture hours:

i. **Introduction to Computer Organization:** Notion of organization and architecture. Von Neumann and Harvard architectures. Evolution of computers. Role of VLSI Technology in miniaturization of computers. **1 hour**

ii. **Computer System Design:** Introduction, design of a computer system, register transfer level (RTL) structure realizing behaviour expressed in an algorithm, logic circuit level structure of RTL components, HDL description of RTL structures at architectural and logic levels. **2 hours**

iii. **Datapath Design:** Block diagram description of a processor, overview of basic digital building blocks in the data-path, adder, subtracter, shifter, multiplier and divider, comparator circuits, optimization of adders and multipliers, integration of arithmetic logic unit, design of general purpose register files in RISC and CISC processors, integration of data-path using ALU and general purpose register file, integer versus floating point ALU, IEEE 754 single precision, double precision and extended double precision floating point formats, algorithms and RTL realization of floating point adders, subtractors, multipliers, dividers, design of floating point ALU. **8 hours**

iv. **Controller Design:** Motivation behind use of controller circuits, instruction interpretation and execution, design of hardwired controller based on finite state machine model, design of microprogrammed control circuits, horizontal and vertical microprogramming, integration of controller and data-path into a processor, design of RISC and CISC processors, examples of some well-known processors. **5 hours**

v. **Instruction set architecture and addressing modes:** Concept of instruction formats, types of instructions, different types of addressing modes, programming considerations in

register transfers and assembly languages. Example case study of ARM processor including its instruction formats and addressing modes. Assembly language programming of ARM processor. **5 hours**

vi. **Memory organization and design:** Introduction, processor-memory interaction, storage technology, memory array organization and technology, semiconductor memories, ROM, static and dynamic RAM, 1D, versus 2D RAM, FPMDRAM, EDODRAM, SDRAM, RDRAM, DDRRAM, DDR2RAM, DDR4RAM, content addressable memory (CAM), memory hierarchy, cache organization, cache coherence protocols, cache mapping techniques – direct, associative, set-associative and sector mapping techniques, cache optimization techniques, virtual memory, multiple module memory, gap filler memories – magnetic bubble memories and charge coupled devices, secondary storage device, disk recording methods, disk drives and controllers, cyclic redundancy check logic. **8 hours**

vii. **Input Output organization:** Introduction, data transfer techniques, bus interface, programmed I/O, interrupt driven I/O, conflict resolution of interrupts, programmable interrupt controller, direct memory access (DMA), DMA controller, types of DMA. **5 hours**

viii. **Pipelining:** Linear pipelined architectures, synchronous versus asynchronous pipelining, non-linear pipelining, reservation and latency analysis, collision free scheduling, pipeline schedule optimization. **4 hours**

ix. **Multiprocessor architectures:** Flynn's classification of computers, SISD, SIMD, MISD and MIMD architectures, shared memory multiprocessors, distributed memory multicomputers, distributed coherent caches. **4 hours**

3. Laboratory/practical/tutorial Modules:

i. **Hardware description language:** Introduction to some HDL (Verilog, VHDL, BSV). Digital Design using HDLs. Modeling and simulation of ALU, controller and processors using HDL. Timing analysis of processors with inertial and transport delays.

ii. **Assembly language programming:** The assignments should cover the following concepts: Registers, different type of instructions (load, store, arithmetic, logic, branch); operand addressing modes; memory addressing modes; conditions (codes/flags and conditional branches) stack manipulation; procedure calls; procedure call conventions (load/store of; arguments on stack, activation records)

iii. **Realization of Computer Circuits:** Realization of arithmetic and logic circuits on bread board, realization of memory and I/O interface circuits on bread board, study of universal synchronous-asynchronous receiver transmitter on bread board.

4. Text books:

i. V. Carl Hamacher, Zvonko G. Vranesic, Safwat Zaky, "Computer Organization", 5th Edition, Mc Graw Hill Education, July 2017.

5. References:

i. John P. Hayes, "Computer Organization and Architecture", 3rd Edition, Mc Graw Hill Education, July 2017.

ii. William Stallings, "Computer Organization and Architecture", 11th Edition, Pearson Education, 2022.

iii. Zainalabedin Navabi, "VHDL: Modular Design and Synthesis of Cores and Systems", 3rd Edition, Mc Graw Hill Education, 2022.

iv. **Similarity with the existing courses:**
(Similarity content is declared as per the number of lecture hours on similar topics)

S. No.		Course Code	Similarity Content	Approx. % of Content
1.	Computer Organization	CS201	Modules i, ii, vii, viii, ix in full and iii, iv, v, vi in part	67%

6. Justification of new course proposal if cumulative similarity content is >30%:

The B.Tech (CSE) students study a core course on Computer Organization (CS201) in which they study the content at a considerable higher level of abstraction where they do not enter into the details of computer design, computer circuits, etc. However, B.Tech (EE) students need to study Computer Organization from a designer's perspective with special emphasis to computer circuits. Hence, we propose a separate course on Computer Organization and Processor Architecture Design as a core course specifically for B.Tech (EE) students.